Abstract of the Disclosure

Described herein is a system for verifying that a circuit described by a hardware description language file has a property of responding to an antecedent event represented by a particular pattern in its input signals by exhibiting a consequent behavior of producing a particular pattern in its output signals during a finite time following the antecedent event. The system includes a conventional circuit simulator for simulating the behavior of the circuit under conditions defined by a user-provided test bench. The simulator produces output waveform data representing the behavior of the circuit input, output and internal signals, including signals representing the circuit's state. When the output waveform data indicates the antecedent event has occurred, the system determines the current state of the circuit from the waveform data. The system then creates and analyzes a temporally expanded model of the circuit to verify whether, starting from that current state, the circuit will exhibit the consequent behavior within that finite time under all input signal conditions.